CLAIMS:

1. A semiconductor memory device comprising:

a memory cell unit having a plurality of memory cells connected in series and having a first end and a second end;

a first select transistor connected to the first end of said memory unit;

a second select transistor connected to the second end of said memory unit; and

a programming circuit which programs a selected memory cell among said plurality of memory cells, wherein

said programming circuit applies, at a time of programming, a first voltage to a gate electrode of the selected memory cell, applies a second voltage to a gate electrode of a memory cell positioned between the selected memory cell and the second end and adjacent to said selected memory cell, the second voltage being lower than the first voltage, applies a third voltage to a gate electrode of at least one memory cell between a memory cell, to which the second voltage is applied, and the second end, the third voltage being lower than the first voltage but higher than the second voltage, and applies a fourth voltage to a gate electrode of a memory cell positioned between a memory cell adjacent to said selected memory cell and the first end, the fourth voltage being lower than the first voltage but higher than the second voltage.

2. The device according to claim 1, wherein the second voltage is a ground voltage.

3. The device according to claim 1, wherein the third voltage has a same voltage as the fourth voltage.

4. The device according to claim 1, wherein the second voltage is a ground voltage, and the third voltage has a same voltage as the fourth voltage.

5. A semiconductor memory device comprising:

a memory cell unit having a plurality of memory cells connected in series and having a first end and a second end;

a first select transistor connected to the first end of said memory unit;

a second select transistor connected to the second end of said memory unit;

a bit line connected to said memory unit via said first select transistor; and

a programming circuit which programs a selected memory cell among said plurality of memory cells, wherein

said programming circuit applies, at a time of programming, a first voltage to a gate

electrode of the selected memory cell, applies a second voltage to a gate electrode of a memory cell positioned between the selected memory cell and the second end and adjacent to said selected memory cell, the second voltage being lower than the first voltage, applies a third voltage to a gate electrode of at least one memory cell, to which the second voltage is applied, and the second end, the third voltage being lower than the first voltage but higher than the second voltage, applies a fourth voltage to a gate electrode of a memory cell positioned between a memory cell adjacent to said selected memory cell and the first end, the fourth voltage being lower than the first voltage but higher than the second voltage, applies a fifth voltage to a gate electrode of the first select transistor, the fifth voltage being higher than the second voltage but lower than the third and fourth voltages, and applies a sixth voltage to the bit line while keeping the second select transistor at a non-conductive state, the sixth voltage being dependent on data to be programmed into the selected memory cell.

6. The device according to claim 5, wherein the second voltage is a ground voltage.

7. The device according to claim 5, wherein the third voltage has a same voltage as the fourth voltage.

8. The device according to claim 5, wherein the second voltage is a ground voltage, and the third voltage has a same voltage as the fourth voltage.

9. The device according to claim 5, wherein the sixth voltage has a same voltage level as the fifth voltage when the selected memory cell is not programmed.

10. The device according to claim 5, wherein, both of the third voltage and the fourth voltage are applied to the gate electrodes of remaining memory cells prior to applying the first voltage to the gate electrode of the selected memory cell.

11. The device according to claim 5, wherein the sixth voltage is applied to the bit line prior to applying the first voltage to the gate electrode of the selected memory cell and applying the third voltage and the fourth voltage to the gate electrodes of remaining memory cells.